2818

Attorney's Docket No.: 03692.P059DC **Patent**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

DISNEY, D.

Serial No.: 10/722,792

Filing Date: November 25, 2003

For: **METHOD OF FABRICATING A HIGH-VOLTAGE TRANSISTOR WITH A MULTI-LAYERED EXTENDED DRAIN STRUCTURE**

Examiner: Nhu, David

Art Unit: 2818

Information Disclosure Statement

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Enclosed is a copy of Information Disclosure Citation Form PTO-1449A together with a copy of the documents cited on that form. It is respectfully requested that the cited documents be considered and that the enclosed copy of Information Disclosure Citation Form PTO-1449A be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s). Applicant also wishes to bring to the attention of the Examiner the related divisional application Serial no. 10/278,551 (issue fee paid 11/25/03).

Pursuant to 37 C.F.R. § 1.97, the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made and is not to be construed as an admission that the information cited in this statement is material to patentability.

Pursuant to 37 C.F.R. § 1.97, this Information Disclosure Statement is being submitted under one of the following (as indicated by an "X" to the left of the appropriate paragraph):

_____ 37 C.F.R. §1.97(b).

__XX__ 37 C.F.R. §1.97(c). If so, then enclosed with this Information Disclosure Statement is one of the following:

____ A statement pursuant to 37 C.F.R. §1.97(e) or

__X__ A check for $180.00 for the fee under 37 C.F.R. § 1.17(p).

_____ 37 C.F.R. §1.97(d). If so, then enclosed with this Information Disclosure Statement are the following:

(1) A statement pursuant to 37 C.F.R. §1.97(e); and

(2) A check for $180.00 for the fee under 37 C.F.R. §1.17(p) for submission of the Information Disclosure Statement.

Respectfully submitted,

BURGESS & BEREZNAK, LLP

Dated: April 10, 2004

Bradley J. Bereznak
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FIRST CLASS CERTIFICATE OF MAILING
(37 C.F.R. § 1.8(a))

I hereby certify that the foregoing Information Disclosure Statement, together with Form PTO-1449A and one copy of each reference as cited therein, are being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on April 09, 2004.

Caitlin R. Burgess
Name of Person Mailing Correspondence

Signature

4-09-04
Date

Form PTO-1449 (Modified)	Atty Docket No.: 03692.P059DC	Serial No.: 10/722,792
List of Patents and Publications Statement (Use several sheets if necessary)	Applicants: Disney, D.	
	Filing Date: November 25, 2003	

REFERENCE DESIGNATION | **U.S. PATENT DOCUMENTS**

Exam. Initial		Date	Document Number	Name	Class	Sub-Class	Filing Date

FOREIGN PATENT DOCUMENTS

No.		Document No.	Date	Country	Name	Class	Sub-Class	Trans-lation
		JP 56-38867	04/14/81	Japan	Okabe, T., et al.			English
		JP 57-10975	01/20/82	Japan	Sanyo			
		W/O 99/34449	07/08/99	PCT	Konin Klijke			
		JP 57-12557	01/22/82	Japan	Tanaka, T., et al.			
		JP 57-12558	01/22/82	Japan	Tanaka, T., et al.			
		JP 60-64471	04/13/85	Japan	Saiotou, M.			
		JP 3-211771	09/17/91	Japan	Toshiba			

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

		International Electron Device Meeting 1979 – Washington, D.C., Dec. 3-4-5, Sponsored by Electron Devices Society of IEEE, Pages 238-241
		"Realization of High Breakdown Voltage (>700V) in Thin SOI Devices" S. Menchant, et al., Phillips Laboratories North American Phillips Corporation 1991 IEEE, Pages 31-35

Examiner	*Date Considered*

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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No.		**Document No.**	**Date**	**Country**	**Name**	**Class**	**Sub-Class**	**Trans-lation**
		JP 4107877A	04/09/92	Japan	Yamanishi, et al.			
		JP 6-224426	08/12/94	Japan	Uno, et al.			English
		DE 43 09 764	09/29/94	Germany	Tihanyi, et al.			
		JP 04-107867	08/12/94	Japan	Kawasaki, et al.			
		JP 2000-349288	12/15/00	Japan	Ueno			English
		W/O 97 35346	11/25/97	PCT	Tihanyi			
		W/O 00 33385	06/08/00	PCT	Tihanyi			
		W/O 02 41402	05/23/02	PCT	Baliga, et al.			

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

		"Theory of Semiconductor Superjunction Devices," Fujihira, Japan Journal of Applied Physics Part 1, October 1997, Vol. 36, No.10, Pages 6254-6262
		"Air-Gap Formation During IMD Deposition to Lower Interconnect Capacitance," B. Shieh, K.C. Sanaswat IEEE Electron Device Hettas, Vol. 19, No. 1, Jan. 1998

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No.		Document No.	Date	Country	Name	Class	Sub-Class	Trans-lation
		W/O 02 099909	12/12/02	PCT	Liang, et al.			
		EP 1073 123 A2	07/28/00	EP	Yasuhara			
		GB 2 309 336 A	01/21/97	UK	Fujihira			

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

		"Oxide-Bypassed VDMOS (OBVDMOS): An Alternative to Superjunction High-Voltage MOS Power Devices," Yung C. Liang, et al., August 2001, IEEE Electron Device Letters Vol. 22, No. 8, Pages 407-409
		"Comparison of High-Voltage Devices for Power Integrated Circuits," R. Jay Anaman, et al., IEDM 84, Pages 258-261
		"A New Generation of High-Voltage MOSFET's Breaks the Limit Line of Silicon," G. Debby, et al., Siemens AG, Semiconductor Division, Munchen, Germany; IEDM 98-683 to IEDM 98-685

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OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

		"High Performance 600V Smart Power Technology Based on Thin Layer Silicon-on-Insulator," T. Levatic, et al., Philips Research, Philips Electronics North America Corporation, 4 Pages.
		"Modern Semiconductor Device Physics," S.M. Sze, John Wiley & Sons, Chapter 4 ("Power Devices") pp.203-206, (1998)
		"Modeling Optimization of Lateral High-Voltage IC Devices to Minimize 3-D Effects," Hamza Yilmaz, R&D Engineering, Semiconductor Business Division, General Electric Company, NC, pp. 290-297
		"Optimization of the Specific On-Resistance of the COOLMOS™," Chen, et al., IEEE Transactions on Electronic Devices, Vol. 48, no. 2, February 2001

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		"Lateral Unbalanced Super Junction (USJ) / 3D-RESURF for High Breakdown Voltage on SOI," Ng, et al., pp. 395-398, 04/06/2001
		"Static and Dynamic Electricity," William R. Smythe, McGraw-Hill Book Company, Inc., New York, 1950.

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